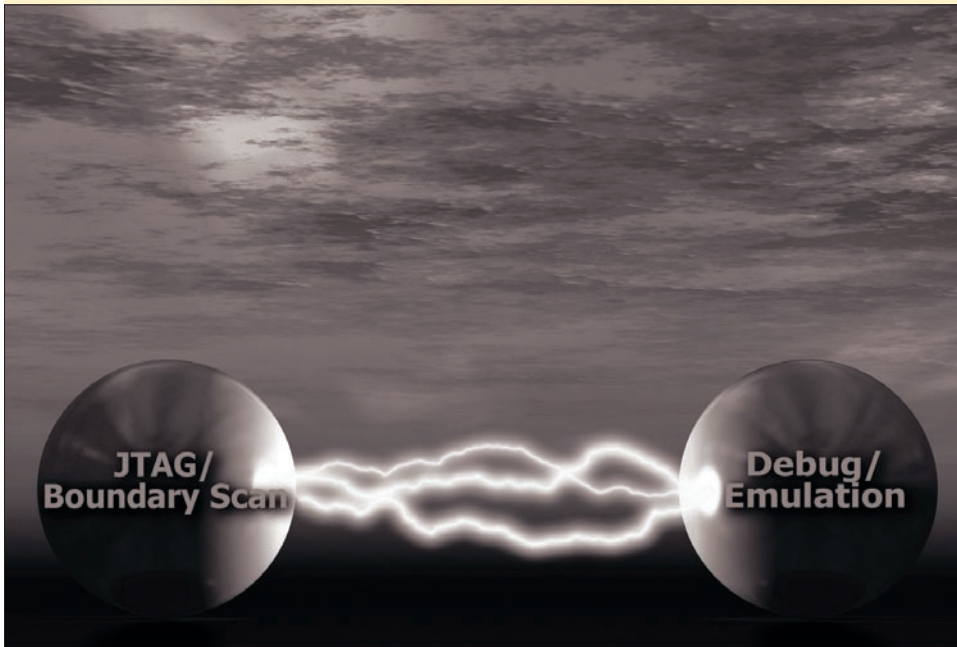
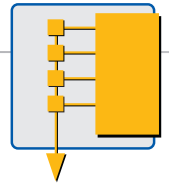


The Fusion of JTAG Emulation and Boundary Scan Test

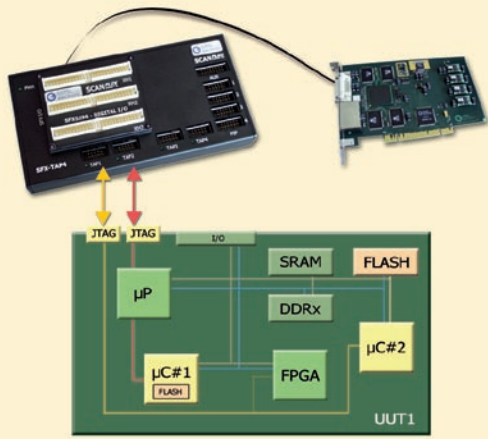


The new tools are fully integrated into SYSTEM CASCON™



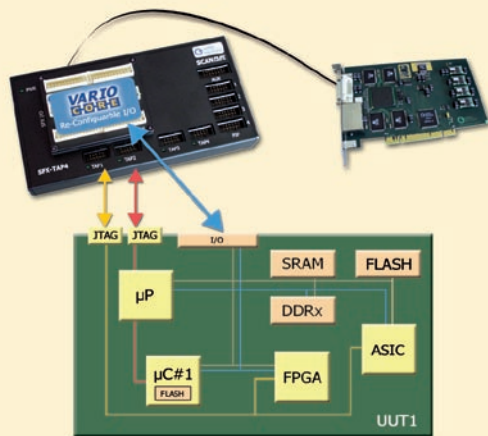
- Single, integrated platform for emulation and JTAG/Boundary Scan
- No additional hardware required
- Ultra-fast programming for on-chip and external Flash
- Functional and at-speed testing of non-Boundary Scan devices
- Interlaced emulation and Boundary Scan Test
- Extension of SYSTEM CASCON™ and integrated with **SCANFLEX**

VarioTAP® is based on special device models and is tightly integrated in the development environment SYSTEM CASCON™, no other tools tailored to the target μ P are needed. VarioTAP® functions for debug/emulation, in-system programming and test are available for implementation in CASLAN programs and will allow automated generation of interlaced emulation and test vectors.



Example 1

VarioTAP® scenario for programming of an on-chip Flash and an external Flash with two different µC on a UUT (single board).



Example 2

VarioTAP® scenario for test of a UUT with two chains, including external I/O (single board), plus on-chip ISP for Flash inside µC#1.

Key Advantages and Features

A single platform solution for emulation and JTAG/Boundary Scan, VarioTAP®, is a revolutionary technology for pattern streaming on TAP (Test Access Port) signals compliant with IEEE-Std.1149.1. The technology utilizes on-chip debug/emulation resources accessible in most microprocessors and microcontrollers through a IEEE 1149.1 compatible JTAG port. The VarioTAP® principle was specifically developed for the integrated Boundary Scan software, SYSTEM CASCON™, and enables the complete fusion of debug/emulation tools with test and in-system programming (ISP) applications. The VarioTAP® specific adaptive streaming demonstrates the dynamic synthesis of emulation vectors and Boundary Scan vectors, supporting new test strategies such as Interlaced JTAG/Boundary Scan Tests and in-system emulation test/ISP.

- Automated support of Scan Router devices
- Support of multiprocessor/multicore systems with single or multiple TAPs
- Same user interface for both emulation and JTAG/Boundary Scan

Comprehensive Fault Coverage

- Functional and at-speed test of non-Boundary Scan devices
- Comprehensive test coverage of dynamic RAM (e.g. DDR2/DDR3)
- Fast generation of custom tests without the native tools for each µP family

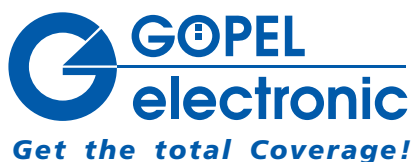
Ease of Programming

- Ultra-fast programming of on-chip and external Flash
- Simplified GUI utilizing VarioTAP® models with pre-configured IP
- Production quality hardware interface

SCANFLEX® supports up to eight independent, truly parallel TAPs (JTAG/debug/emulation ports). The TAP of a µP to be controlled with VarioTAP® can be freely assigned to any of the Boundary Scan controller TAPs. The scan chain may contain other devices and can even be part of a multi-drop or hierarchical scan path configuration.

GOEPEL electronics Ltd.
 Unit 1A, The Old Granary
 Westwick
 Cambridge
 CB24 3AR
 United Kingdom
 Phone: +44 (0) - 1223 - 858 - 298
 Fax: +44 (0) - 8451 - 309 - 004

GOEPEL electronics LLC
 9600 Great Hills Trail
 Suite 150 W
 Austin, TX 78759
 United States of America
 Phone: +1 (0) - 512 - 502 - 3010
 Fax: +1 (0) - 512 - 502 - 3076



ISO 9001 certified

GOEPEL electronic GmbH
 Goeschwitzer Str. 58/60
 D - 07745 Jena
 Phone: +49 (0) - 3641 - 6896 - 0
 Fax: +49 (0) - 3641 - 6896 - 944
 E-Mail: sales@goepel.com
 Internet: www.goepel.com

Authorised Distributor: